Google

Web Images Groups News Froogle Local **more »**

place and route array context compiler   Search   Advanced Search
                                                                 Preferences

The **"AND"** operator is unnecessary – we include all search terms by default. [details]

Web

Results **1 - 10** of about **568,000** for **place** and **route array context compiler**. (0.31 seconds)

Ultra-Fast Automatic Placement for FPGAs (ResearchIndex)
... Gate **Array** FPGA **compilation** tools has escalated for three reasons first, ...
18 New Algorithms for **Placement** and **Routing** of Macro Cells **(context)** ...
citeseer.ist.psu.edu/sankar99ultrafast.html - 26k - Cached - Similar pages

ACRES Architecture and Compilation (ResearchIndex)
31 Architecture of FieldProgrammable Gate **Arrays (context)** - Rose, Gamal et al.
- 1993 ... 4 Fast and Efficient **Place** and **Route** for Pipeline Reconfigurab. ...
citeseer.ist.psu.edu/ang04acres.html - 31k - Cached - Similar pages
[More results from citeseer.ist.psu.edu]

Reconfigurable computing - Wikipedia, the free encyclopedia
Obtained after **place** and **route**, final.result of the **place** and **route** phase. ...
Often the reconfigurable **array** is used as a processing accelerator attached ...
en.wikipedia.org/wiki/Reconfigurable_system - 39k - Cached - Similar pages

[PDF] Zippy - A coarse-grained reconfigurable **array** with support for ...
File Format: PDF/Adobe Acrobat
erated using the Zippy **place** and **route** tools. Figure 4. shows that for this
implementation ... a coarse-grained multi-**context** reconfigurable **array**. A dis- ...
doi.ieeecomputersociety.org/10.1109/ASAP.2005.69 - Similar pages

[PDF] Fast Area Estimation to Support **Compiler** Optimizations in FPGA ...
File Format: PDF/Adobe Acrobat
HLL Program. **Compiler** & Optimizations. (msec to sec). Y. **Place & Route**. (minutes to
... In this **context**, resources are defined to be the ...
doi.ieeecomputersociety.org/10.1109/FPGA.2002.1106678 - Similar pages

[PDF] What Is a **Compiler** When The What Is a **Compiler** When The ...
File Format: PDF/Adobe Acrobat - View as HTML
Multi-**context**. Reconfigurable Logic. **Array**. **Array** Register File ... **Place** and
route inherently complex. • Would like to have **compile** times of the order of ...
www.crest.gatech.edu/publications/utah2001.pdf - Similar pages

[PPT] PowerPoint-Präsentation
File Format: Microsoft Powerpoint 97 - View as HTML
place & route tools. fully parameterized to support all Zippy architecture ...
Virtualizing Hardware with Multi-**Context** Reconfigurable **Arrays Arrays** ...
www.tik.ee.ethz.ch/~plessl/publications/asap05/asap05.ppt - Similar pages

Transit Note #119 D/FPGAs in an ASIC Core Cell Methodology
Once the **array** is generated, the **compiled array** should, in fact, ... from core
or memory blocks to the vendor's backend **placement** and **routing** process. ...
www.cs.caltech.edu/research/ic/transit/tn119/tn119.html - 10k - Cached - Similar pages

[PDF] Classification of **Compiler** Optimizations for High Performance ...
File Format: PDF/Adobe Acrobat - View as HTML
optimizations focus on more partitioning, **placement** and **route** of memories and
... backend **compiler** can assign some of the **arrays** to these available on-chip ...
www.docm.mmu.ac.uk/STAFF/A.Nisbet/PAPERS/fpga_opt.pdf - Similar pages

[PDF] Incremental **compilation** for parallel logic verification systems ...
File Format: PDF/Adobe Acrobat - View as HTML
field-programmable gate-**array**-based Ikos VirtuaLogic emulator. [1]. The modified
compiler ... processor **compilation** (eg, FPGA **place** and **route**), which can ...
www.ecs.umass.edu/ece/tessier/tvlsi-increment.pdf - Similar pages

Try your search again on Google Book Search
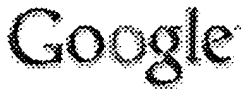
Google

Web   Images   Groups   News   Froogle   Local   more »

place and route array context compiler   [Search]   Advanced Search
                                                      Preferences

The "AND" operator is unnecessary – we include all search terms by default. [details]

Web

Results **11 - 20** of about **568,000** for **place and route array context compiler**. (0.15 seconds)

FPL 2001
Gambit: A Tool for the Simultaneous **Placement** and Detailed **Routing** of Gate-**Arrays**.
243-253 Electronic Edition (link) BibTeX ...
www.informatik.uni-trier.de/~ley/db/conf/fpl/fpl2001.html - 47k - Cached - Similar pages

[PDF] Synthesis and Estimation of Memory Interfaces for FPGA-based ...
File Format: PDF/Adobe Acrobat - View as HTML
successfully in the **context** of a **compiler** that maps. applications directly to
FPGA [1]. ... with a medium effort for **place** and **routing** on a 800 MHz ...
www.isi.edu/~pedro/PUBLICATIONS/ParkDiniz.fccm2003.abst.pdf - Similar pages

[PDF] A Compiler Framework for Mapping Applications to a Coarse-Grained ...
File Format: PDF/Adobe Acrobat
The **compiler** uses a greedy **place**-. and-**route** algorithm to map these pipe stages
onto the ... RC **Array Context**. Configurations. Figure 5: Flow of **Compilation** ...
portal.acm.org/ft_gateway.cfm?id=502235&type=pdf - Similar pages

EETimes.com
Figure 1 depicts the current FPGA design process **context**: using ... After **placement**,
PPR proceeded to **route**. In this design, two time specs were usedone ...
www.eetimes.com/editorial/1996/fpgafeature9601.html - 80k - Cached - Similar pages

[PDF] Dr. José L. Muñoz
File Format: PDF/Adobe Acrobat - View as HTML
FPGA FPGA. **Compiler**. Mapper. Estimator. C. VHDL/Verilog. **Place**. &. **Route**.
Simulation. ACS Program ... ACS RISC + Reconfigurable **Array** architectures entering ...
ehw.jpl.nasa.gov/events/nasa_eh/papers/ACS-EH99-JoseMunoz.pdf - Similar pages

picoChip - picoChip - Frequently Asked Questions
... it doesn't matter: you write the code, **compile** it and **place** in **array**. ...
For FPGAs that provide the same functionality the **place** and **route** time is ...
www.picochip.com/technology/faq - 37k - Cached - Similar pages

Michigan Land Use Institute: Making Smart Growth a Reality In Michigan
New **Route** to Transportation Design Michigan prepares to harmonize highway, ...
"**Context**-sensitive design can help ensure that the cookie-cutter four-lane ...
www.mlui.org/pageview.asp?fileid=16681 - 62k - Cached - Similar pages

Transit Note #112 DELTA: Prototype for a First-Generation ...
Each **array** element contains its own memory block to store individual configuration
bits, where each set of configuration is a ``**context**'' programmed to ...
www.cs.caltech.edu/research/ic/transit/tn112/tn112.html - 26k - Cached - Similar pages

Comprehensive solution enables high-performance FPGA design
To improve throughput and the distribution of design tasks, an intuitive mechanism
to **compile** the necessary vendor libraries for post-**place-and-route** ...
dataweek.co.za/news.asp?pklNewsId=16201&pklIssueId=524&pklCategoryID=35 - 41k - Cached - Similar pages

Algorithmic and Theoretical Problems Related to the Physical ...
51 The Timberwolf **Placement** and **Routing** Package (**context**) - Sechen,
Sangiovanni-Vincentelli - 1985 44 A Detailed Router for Field-Programmable Gate **Arrays** ...
citeseer.ifi.unizh.ch/karro00algorithmic.html - 32k - Cached - Similar pages

◀ Goooooooooooogle ▶

-

-

place and route array context com Search

Search within results | Language Tools | Search Tips

Google Home - Advertising Programs - Business Solutions - About Google

©2006 Google

Google

Web   Images   Groups   News   Froogle   Local   more »

place and route matrix mapping PE   Search   Advanced Search
                                                   Preferences

The "AND" operator is unnecessary -- we include all search terms by default. [details]

Web

Results **1 - 10** of about **571,000** for place and route matrix mapping PE. (0.31 seconds)

[PDF] Floating-Point Sparse **Matrix**-Vector Multiply for FPGAs pdfauthor
File Format: PDF/Adobe Acrobat - View as HTML
PE Place. Schedule. Computation. Schedule. Communication. Assemble. Memories.
Computation &. Communication. Memories. **Matrix** Mapper. Figure 8: **Matrix Map** ...
www.cs.caltech.edu/research/ic/pdf/smvm_fpga2005.pdf - Similar pages

[PDF] Network Topology Exploration of Mesh-Based Coarse-Grain ...
File Format: PDF/Adobe Acrobat - View as HTML
an operation to **PE mapping** technique that exploits tempo-. ral locality between
operations by **mapping** operations with ... Fast and efficient **place** and **route** ...
www.cecs.uci.edu/~sumitg/pubs/CoreComp-TopExplore-Date04.pdf - Similar pages

[PDF] Network Topology Exploration of Mesh-Based Coarse-Grain ...
File Format: PDF/Adobe Acrobat - View as HTML
scheduling, operation to **PE** binding (or **mapping**), and **routing** problems. ... Fast and
efficient **place** and **route** for pipeline reconfigurable architectures. ...
www.cecs.uci.edu/technical_report/TR03-27.pdf - Similar pages

[PDF] Thermal-aware IP virtualization and **placement** for networks-on-chip ...
File Format: PDF/Adobe Acrobat - View as HTML
Wong used **matrix** synthesis problem (MSP) to model the. thermal **placement** problem
and three ... decoupled from its physical **PE mapping** in the previous ...
www.cse.psu.edu/~whung/iccd2004.pdf - Similar pages

[PDF] Microsoft PowerPoint - MPSoC04_presentation_wehn.ppt
File Format: PDF/Adobe Acrobat - View as HTML
Access Pattern must be stored for each interleaver/**matrix**. Flexibility costs a huge
amount of ... (no **place & route**). x 1.6. Design Effort. 2 **MAP** units ...
tima.imag.fr/mpsoc/2004/slides/Wehn.pdf - Similar pages

[PDF] 4. Programming of Coarse Grain Reconfigurable Platforms
File Format: PDF/Adobe Acrobat - View as HTML
are the PADDI-2, the **MATRIX**, and, as reconfigurable coprocessors, the REMARC ...
mapping and **placement** in one step and a simple greedy **routing** algorithm. ...
xputers.informatik.uni-kl.de/papers/publications/Nageldinger4.pdf - Similar pages

Xcell Journal Online -- Bioinformatics article - Issue 53
FPGA I/O ports for the whole design can be **mapped** to the device pins using the
high-level ... and the **place** and **route** timing netlist is generated. ...
www.xilinx.com/publications/xcellonline/xcell_53/xc_bioinfo53.htm - 38k -
Cached - Similar pages

TechOnLine - Reconfigurable Processors: Changing the Systems ...
The first differentiation we experienced with the reconfigurable processor solution over
FPGAs solution was the deterministic **place** and **route**. We could **map** ...
www.techonline.com/community/ed_resource/feature_article/38022 - 36k -
Cached - Similar pages

[PDF] Energy/Power Estimation of Regular Processor Arrays
File Format: PDF/Adobe Acrobat - View as HTML
As seen in 2.1, we obtain a 2D **pe** array from the **mapping**. step. Hence two single
hyperplanes ... computation time (for **place** and **route**) on a recent work- ...
www.irisa.fr/cosi/HOMEPAGE/Derrien/publi/ISSS-02.pdf - Similar pages

[PDF] Combined Instruction and Loop Parallelism in Array Synthesis for FPGAs
File Format: PDF/Adobe Acrobat - View as HTML
moved into the **pe** data-path using standard commerecial. circuit retimers. Our
experiments (based on performance es-. timates after **place-and-route**) have ...

Web   Images   Groups   News   Froogle   Local   more »

Google   place and route matrix mapping FPGA   Search   Advanced Search
Preferences

The "AND" operator is unnecessary -- we include all search terms by default. [details]

Web   Results 1 - 10 of about **84,800** for **place** and **route** **matrix** **mapping** FPGA. (0.26 seconds)

[PDF] **Routing**-directed **Placement** for the T FPGA
File Format: PDF/Adobe Acrobat - View as HTML
matrix. **FPGA mapping** begins by dividing the circuit. into pieces of sequential logic

[PDF] Dynamic **FPGA Routing** for Just-in-Time **FPGA** Compilation
File Format: PDF/Adobe Acrobat - View as HTML
technology **mapping** and VPR's bounding box **placement**. However, incorporating
existing **FPGA routing** algorithms within. a JIT compiler is not possible given ...
www.cecs.uci.edu/conference_proceedings/dac_2004/lysecky_dynamic.pdf -
Similar pages

[PDF] Dynamic **FPGA Routing** for Just-in-Time **FPGA** Compilation
File Format: PDF/Adobe Acrobat - View as HTML
and execute technology **mapping, placement**, and **routing**. Such. compilation would be
done on a small lean processor coexisting. on the **FPGA** for this purpose, ...
www.cs.ucr.edu/~vahid/pubs/dac04_jitfpgaroute.pdf - Similar pages

[PDF] A First Approach to Synthesis from Assembly Code for Hardware ...
File Format: PDF/Adobe Acrobat - View as HTML
the previous switch **matrix** and attempt to **route** the wire in the ... technology **mapping**,
and **place** and **route**. Code Size is the ...
www.cs.ucr.edu/~vahid/pubs/dac03_dhs.pdf - Similar pages

Comparison **Matrix**
LeonardoSpectrum Comparison **Matrix**. ... Integration w/ **FPGA** vendor Floorplanning,
Place & Route Tools. a. a. " Can assign synthesized cells to physical ...
www.mentor.com/products/**fpga**_pld/synthesis/leonardo_spectrum/comp_**matrix**.cfm -
53k - Cached - Similar pages

Reconfigurable computing - Wikipedia, the free encyclopedia
Refers to total on-chip memory available for multi-**FPGA** systems. ... **Place** and **Route**.
Process of converting a netlist into physically **mapped** and **placed** ...
en.wikipedia.org/wiki/Reconfigurable_system - 39k - Cached - Similar pages

Reconfigurable computing - Wikipedia, the free encyclopedia
The XD1 **FPGA** reconfiguration is accomplished via the traditional HDL design ... **Place**
and **Route**. Process of converting a netlist into physically **mapped** and ...
en.wikipedia.org/wiki/Reconfigurable_computing - 39k - Cached - Similar pages

[PDF] **Mapping** multi-mode circuits to LUT-based **FPGA** using embedded MUXes ...
File Format: PDF/Adobe Acrobat
Mapping multi-mode circuits to LUT-based **FPGA** using embedded MUXes. Tim
Courtney, Richard Turner, ... This was then changed to 35MHz for **place & route**. ...
doi.ieeecomputersociety.org/10.1109/FPGA.2002.1106699 - Similar pages

[PDF] PAM-Blox : High Performance **FPGA** Design for Adaptive Computing ...
File Format: PDF/Adobe Acrobat
fers an integrated **FPGA** design system with **placement** hints. at the design entry level. ...
technology **mapping** to **place** and **route**. Trianus is currently ...
doi.ieeecomputersociety.org/10.1109/FPGA.1998.707894 - Similar pages

List of **FPGA**-based Computing Machines
FPGA Devices for Data Processing/**Routing**/Switching:: 32 XC4000E(X)s ... 100%
automatic **place** and **route**. System compiles in under ten seconds per chip. ...
www.io.com/~guccione/HW_list.html - 132k - Cached - Similar pages